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APPLICATION NO.	FI	LING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/790,450	(02/27/2004 Jinichi Morimura 112857-474		9916	
	7590	03/30/2005		EXAM	INER
William E.	Vaughan		ANYA, IGWE U		
Bell, Boyd	& Lloyd LI	.C			
P.O. Box 11	•			ART UNIT	PAPER NUMBER
Chicago II	60690-1	135		2001	

DATE MAILED: 03/30/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant/s)			
	Application No.	Applicant(s)			
Office Action Summary	10/790,450	MORIMURA ET AL.			
Office Action Summary	Examiner	Art Unit			
	Igwe U. Anya	2891			
The MAILING DATE of this communication Period for Reply	appears on the cover sheet with	the correspondence address			
A SHORTENED STATUTORY PERIOD FOR RETHE MAILING DATE OF THIS COMMUNICATION - Extensions of time may be available under the provisions of 37 CF after SIX (6) MONTHS from the mailing date of this communication - If the period for reply specified above is less than thirty (30) days, and If NO period for reply is specified above, the maximum statutory period for reply within the set or extended period for reply will, by significant the period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will, by significant the set of extended period for reply will be set of extended period for reply wil	ON. R 1.136(a). In no event, however, may a repin. a reply within the statutory minimum of thirty (eriod will apply and will expire SIX (6) MONTHatute, cause the application to become ABA	oly be timely filed (30) days will be considered timely. HS from the mailing date of this communication. NDONED (35 U.S.C. § 133).			
Status					
1)⊠ Responsive to communication(s) filed on 2	27 February 2004.				
	This action is non-final.				
·=					
closed in accordance with the practice und	·				
Disposition of Claims					
4)⊠ Claim(s) <u>16 and 17</u> is/are pending in the a	oplication				
4a) Of the above claim(s) is/are with	•				
5) Claim(s) is/are allowed.					
6)⊠ Claim(s) <u>16 and 17</u> is/are rejected.					
7) Claim(s) is/are objected to.					
8) Claim(s) are subject to restriction ar	nd/or election requirement.				
Application Papers					
9) The specification is objected to by the Exam	niner	<u>_</u> .			
10)⊠ The drawing(s) filed on <u>27 February 2004</u> is		niected to by the Examiner			
Applicant may not request that any objection to					
Replacement drawing sheet(s) including the co		• •			
11) The oath or declaration is objected to by the	,	, ,			
Priority under 35 U.S.C. § 119					
12) ☐ Acknowledgment is made of a claim for fore	eian priority under 35 U.S.C. & 4	119(a)-(d) or (f)			
a) ☐ All b) ☐ Some * c) ☐ None of:	sign phonty under 55 c.c.c. g	113(a)-(u) 01 (1).			
1.☐ Certified copies of the priority docum	nents have been received.				
2. Certified copies of the priority docum	•	plication No.			
3. Copies of the certified copies of the	•	·			
application from the International Bu		C			
* See the attached detailed Office action for a	list of the certified copies not re	eceived.			
Attachment(s)					
1) X Notice of References Cited (PTO-892)	4) 🔲 Interview Sur	mmary (PTO-413)			
2) 🔲 Notice of Draftsperson's Patent Drawing Review (PTO-948)) Paper No(s)/l	Mail Date			
 Information Disclosure Statement(s) (PTO-1449 or PTO/SB Paper No(s)/Mail Date <u>7/30/04</u>. 	3/08) 5) Notice of Info 6) Other:	ormal Patent Application (PTO-152) -			

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DETAILED ACTION

Claim Rejections - 35 USC § 103

- 1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:
 - (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.
- 2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).
- 3. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murohara (US Patent 6069402) in view of Jarvis (US Patent 5200601).
- 4. Murohara teaches method for manufacturing a semiconductor integrated circuit device comprising the steps of:

forming a plurality of circuit patterns on a substrate (3);

bonding a plurality of semiconductor integrated circuit chips (9) onto a first surface of the substrate having the circuit patterns formed thereon, and connecting

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electrodes (8) of the semiconductor integrated circuit chips to each of the circuit patterns;

applying a first seal resin (1, 5) onto each of the semiconductor integrated circuit chips;

disposing a first reinforcement plate (16) above the first seal resin; applying a second seal resin (1) onto a second reinforcement plate (17); disposing the second reinforcement plate on a second surface of the substrate

with the second seal resin there between (fig. 1);

pressurizing the first and second seal resins via the first and second reinforcement plates so as to let flow the first seal resin along a peripheral faces of each of the semiconductor integrated circuit chips (col. 3 lines 28 – 41);

hardening the seal resins flown along the peripheral faces of the semiconductor integrated circuit chips (col. 3 lines 41 - 66); and

thereafter dividing the substrate into a semiconductor integrated circuit device at every semiconductor integrated circuit chip (col. 4 line lines 3 - 8).

- 5. Murohara lacks a reinforcing plate of metal material (though other materials are suggested in col. 4 lines 16 19).
- However, Jarvis teaches reinforcing plates (7A, 7b) of metal material (col. 2 lines
 48) for good tensile strength.
- 7. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Jarvis into the Murohara reference to manufacture a flexible card.

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8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Murohara (US Patent 6069402) in view of Jarvis (US Patent 5200601), and further in view of Arsenault (US Patent 5579117).

- 9. The Murohara/Jarvis reference teaches the features previously outlined, but lacks: disposing an individually divided semiconductor integrated circuit chip on a roll film and coating the same; heating a thin film on which the semiconductor integrated circuit chip is coated with the thin film; manufacturing a card connected plate in which a plurality of semiconductor integrated circuit chips are connected in line; and dividing the card connected plate into an individual semiconductor integrated circuit card.
- 10. However, Arsenault et al. teach:

disposing an individually divided semiconductor integrated circuit chip (10) on a roll film and coating the same (30);

heating (35) a thin film on which the semiconductor integrated circuit chip is coated with the thin film;

manufacturing a card connected plate in which a plurality of semiconductor integrated circuit chips are connected in line; and

dividing the card-connected plate into an individual (5) semiconductor integrated circuit card (col. 5 lines 39 – 55) for enhanced flexibility.

11. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Arsenault et al. into the Murohara/Jarvis reference to manufacture a flexible card.

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Remarks

12. Prior art made of record and not relied upon, considered pertinent to applicant's disclosure include Hirai et al. (US Patent 6160526), Sato et al. (US Patent 5956601), and Uden (US Patent 4649418).

Contact Information

- 13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Igwe U. Anya whose telephone number is (571) 272-1887. The examiner can normally be reached on M F 8:30am 5:00pm.
- 14. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.
- 15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Igwe U. Anya Examiner Art Unit 2891

IA March 25, 2005